REMARKS

The Office Action mailed February 19, 2009, has been carefully reviewed and these remarks are responsive thereto. No new matter has been added. Claims 1-4, 9-14, 20-24, and 28 are presented for examination upon entry of the present paper. Reconsideration and allowance of the instant application are respectfully requested.

Claim Rejections Under 35 U.S.C. § 112

Claims 21, 24, and 28 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. This rejection is traversed.

The Office Action at pages 2-3 contends that the specification fails to provide sufficient direction to one skilled in the art to make and use the invention, wherein an emulation integrated circuit comprises a second signal inclusion schedule. The Office Action at page 3 correctly indicates that the specification at paragraph [31] describes a message formation and send block having a signal inclusion schedule, and that the specification at paragraph [34] describes a message receive and disassembly block having a signal inclusion schedule. Applicants refer the Office to paragraph [28] and Figure 2a of the instant application, wherein an example emulation IC 104 is illustrated and described; *emulation IC 104 includes a number of message send and receive blocks 216*. Thus, by implication, emulation IC (104) may include more than one signal inclusion schedule since each of (1) message formation and send block, and (2) message receive and disassembly block includes a signal inclusion schedule. Furthermore, paragraphs [43], [47], and [57] and Figures 3-4 describe/illustrate storage units 326a and 326b as each storing a signal inclusion schedule. Accordingly, the specification describes the subject matter recited in the claims in adequate detail to enable one skilled in the art to make and use the inventive features of claims 21, 24, and 28.

Claim 28 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. This rejection is traversed.

The Office Action at page 3 contends that the specification, as originally filed, does not disclose a first and second signal inclusion schedule as being different from one another. Applicants disagree. Paragraphs [43], [47], and [57], and Figure 3 describe/illustrate separate

storage units 326a and 326b, and hence, the potential for different signal inclusion schedules (e.g., written description support is provided for features related to a first signal inclusion schedule and a second signal inclusion schedule being different signal inclusion schedules). Furthermore, paragraph [61] describes that storage units 326a and 326b "may share a common storage unit in storing their *respective* schedules." The use of the term "respective" indicates a potential independence (e.g., a difference) between the schedules.

Based on the foregoing remarks, Applicants request withdrawal of the section 112 rejections.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-3, 9-13, and 20-24 stand rejected 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,265,894 to Reblewski et al. (hereinafter referred to as "*Reblewski*") in view of U.S. Patent No. 6,064,677 to Kappler, et al. (hereinafter referred to as "*Kappler*") and U.S. Pub. No. 2003/0144828 to Lin (hereinafter referred to as "*Lin*"). Claims 4 and 14 stand rejected 35 U.S.C. § 103(a) as being unpatentable over *Reblewski*, in view of *Kappler* and *Lin*, and further in view of U.S. Pub. No. 2003/0053435 to Sindhushayana et al. (hereinafter referred to as "*Sindhushayana*"). Claim 28 stands rejected 35 U.S.C. § 103(a) as being unpatentable over *Reblewski*, in view of *Kappler* and *Lin*, and further in view of U.S. Patent No. 6,198,723 to Parruck et al. (hereinafter referred to as "*Parruck*"). Applicants respectfully traverse these rejections.

Independent claim 1 recites, among other features, "a storage unit comprising a signal inclusion schedule . . . the message comprising a plurality of signals assembled in accordance with the signal inclusion schedule, wherein the signal inclusion schedule selects the plurality of signals from at least one pin when the message is assembled."

The Office Action at page 4 correctly indicates that *Reblewski* fails to describe the above-noted features recited in claim 1 related to a storage unit comprising a signal inclusion schedule. The Office Action at pages 4-5 relies on *Kappler* to allegedly remedy the deficiencies of *Reblewski* in this respect.

The Office Action at pages 5 correctly indicates that *Reblewski* and *Kappler* fail to describe the above-noted features recited in claim 1 related to selecting a plurality of signals

from at least one pin. The Office Action contends that *Lin* at paragraph [0688] remedies the deficiencies of *Reblewski* and *Kappler* in this respect, and further asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the scheduler disclosed in *Lin* with the (*Kappler*-modified) reconfigurable integrated circuit of *Reblewski*. Applicants disagree. Paragraph [0688] of *Lin* is reproduced below:

> **[0688]** In a reconfigurable logic (e.g., FPGA) implementation of the same shift register design, if the clock is directly generated from a primary input, the circuit can be designed so that the low skew network can distribute the clock signal to all the logic elements such that the logic elements will detect the clock edge at substantially the same time. Primary clocks are generated from self-timed test-bench processes. Usually, the primary clock signals are generated in software and only a few (i.e., 1-10) primary clocks are found in a typical user circuit design.

Lin at paragraph [0688] merely describes distributing a clock signal to logic elements such that the logic elements detect an edge of the clock at substantially the same time. Even assuming (without admitting) that taking the clock signal from the primary input in *Lin* can appropriately be analogized to selecting a signal from at least one pin, and more broadly, that the distributing of the clock signal to all the logic elements as described in paragraph [0688] of *Lin* can appropriately be analogized to selecting a plurality of signals from at least one pin as recited in claim 1, the distributed clock signal of *Lin* is not included in the assembled message of *Lin*. Instead, in *Lin*, the (distributed) clock signal merely serves to register/gate the inputs to the logic elements upon an edge of the (distributed) clock signal. As such, notwithstanding whether any combination of *Lin*, *Reblewski* and *Kappler* is proper, *Lin* fails to remedy the deficiencies of *Reblewski* and *Kappler* with respect to claim 1. Accordingly, claim 1 is allowable for at least the foregoing reasons.

Furthermore, as discussed at pages 6-7 of Applicants' *Amendment* filed December 3, 2008, the contents of which are incorporated herein by way of reference, the placing in advance of data into time lines 66a-66e serves as the basis of operation of the alleged signal inclusion schedule of *Kappler*. Accordingly, the Office's proposed modification of the alleged signal inclusion schedule of *Kappler* (or more specifically, the Office's proposed modification of the *Kappler*-modified reconfigurable integrated circuit of *Reblewski*) via the incorporation of *Lin's*

alleged teachings is improper. *See* MPEP § 2143.01 (VI.) (The Proposed Modification Cannot Change The Principle Of Operation Of A Reference). As such, because the proposed modification is improper, claim 1 is allowable for at least these additional reasons.

Independent claims 9, 20, and 24 recite features similar to those described above with respect to claim 1. As such, claims 9, 20, and 24 are allowable for at least reasons substantially similar to those discussed above with respect to claim 1.

The dependent claims are allowable for at least the same reasons as their respective base claims because any of the additional applied references (e.g., *Sindhushayana* and *Parruck*) fail to remedy the deficiencies of *Lin*, *Reblewski* and *Kappler* discussed above.

CONCLUSION

All rejections having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same. Should the Examiner find that a telephonic or personal interview would expedite passage to issue of the present application, the Examiner is encouraged to contact the undersigned attorney at the telephone number indicated below. Applicants look forward to passage to issue of the present application at the earliest convenience of the Office.

Respectfully submitted,
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